REMARKS

Claims 1-68 and 82-94 are cancelled; and claims 69-81 remain pending in the application. Claim 81 is amended to place the claim in independent form. The amendments to claim 81 are supported by the originally-filed application at, for example, original claims 69 and 81, as well as by the text within paragraph 0070, and accordingly do not comprise "new matter".

Applicant acknowledges the Examiner's request for restriction of the claims in the application to either CMOS devices or capacitor constructions, and further acknowledges the prior election of the claims directed toward the CMOS device (claims 69-81). Applicant has cancelled the claims directed toward the capacitor construction (claims 82-94) from the application.

The Examiner indicates that an Information Disclosure Statement filed on October 4, 2004 fails to comply with 37 C.F.R. §1.98(a)(1), for failing to provide a list of all patents, publications or other information submitted for consideration by the Office. Applicant has reviewed the Information Disclosure Statement filed October 4, 2004 and cannot find the specific reason for which such Information Disclosure Statement would fail to comply with 37 C.F.R. §1.98. Applicant notes that there is no requirement to provide U.S. patents, and accordingly Applicant has not provided such patents. Applicant further notes that there is a requirement to provide foreign applications and any listed translations thereof to the Patent Office, and Applicant believes that all such foreign applications and the indicated translations thereof were provided to the Patent Office. However, Applicant is resubmitting

the information disclosure statement of October 4, 2004 with this Response, and is also enclosing copies of all foreign documents and any English translations thereof which Applicant has obtained. If the Examiner believes that the Information Disclosure Statement still fails to comply with 37 C.F.R. §1.98, the undersigned respectfully requests a phone call so that the specific problem with the Information Disclosure Statement can be addressed, and the cited references can be appropriately considered by the Examiner.

The pending claims stand rejected as being unpatentable over Tonti (U.S. Patent No. 6,436,749), Chau (US Publication No. 2003/0129793 A1), Taylor (U.S. Patent No. 6,573,160) and Lee (U.S. Patent No. 6,306,743) in various combinations. Applicant respectfully requests reconsideration of such rejections.

Referring initially to claim 69, such recites a CMOS that includes a first metal-containing material within a PMOS gate and over a dielectric layer, and having a thickness of greater than 20Å; in combination with a second metal-containing material within an NMOS gate and over a dielectric layer and having a thickness of less than or equal to about 20Å. Claim 69 is allowable over the cited references for at least the reason that the references do not disclose or suggest the recited CMOS having a recited thick metal-containing material within a PMOS gate in combination with a thin metal-containing material within an NMOS gate.

The Examiner cites Tonti for showing that it was known in the art to form metal-containing materials in the NMOS gate and PMOS gate of CMOS devices, and cites Chau for showing that metal-containing materials formed within gates could be formed to different thicknesses. The Examiner recognizes that the metal-containing materials shown

within the PMOS gates and NMOS gates of Tonti are of the same thickness in the PMOS gates as in the NMOS gates, but submits that it would be obvious to utilize the teachings of Chau to form the metal-containing materials of Tonti to have different thicknesses than those shown.

Applicant respectfully submits that the Examiner's conclusions regarding the teachings of the combined references of Tonti and Chau are mistaken. Tonti describes a process in which a common metal layer (layer 16 of Tonti's Figs. 1-4, for example) is incorporated into NMOS and PMOS devices of CMOS constructions. Since a common metal layer is utilized in the fabrication of the NMOS and PMOS devices of Tonti, the metal layer has a uniform thickness within the NMOS and PMOS devices. Use of the single uniform-thickness metal-containing layer 16 for fabrication of both NMOS and PMOS devices provides a relatively streamlined processing sequence for forming the devices of Tonti as shown in Figs. 1-4. Specifically, the uniform-thickness metal-containing material is patterned simultaneously with an underlying conductively-doped material to form the NMOS and PMOS devices. Any processing which would be included in Tonti to form the metal-containing material 16 to have a different thickness over the NMOS regions than over the PMOS regions would impose additional processing steps to Tonti, which would reduce the efficiency of the Tonti process. Accordingly, it is not obvious to form the layer 16 of Tonti to be a metal-containing layer having different thicknesses over PMOS regions than over NMOS regions, rather than having the uniform thickness shown in Tonti, and accordingly it would not be obvious to modify the teachings of Tonti to generate the claim 1

recited CMOS structure having a metal-containing material within a PMOS gate that is thicker than the metal-containing material within an NMOS gate.

The examiner is correct in noting that the teachings of Chau show metal-containing materials within transistor gates having different thicknesses. However, it is incorrect to assume that such teachings imply a motivation to utilize metal-containing materials within the CMOS structures of Chau having different thicknesses in PMOS regions than in NMOS regions. In fact, neither of the Examiner's cited references of Tonti or Chau suggests or discloses formation of CMOS structures having different thicknesses of metal-containing material within PMOS regions than in NMOS regions, or suggests or discloses any reason why it would be advantageous to form different thicknesses of metal-containing materials within PMOS regions than in NMOS regions. The only of the two references which shows a metal-containing material incorporated into PMOS and NMOS regions of a CMOS (Tonti) specifically shows that the metal-containing material has the same thickness in PMOS regions as in NMOS regions, and has a streamlined manufacturing process which would be more complicated (i.e. less efficient) if it were somehow altered to form the shown uniform-thickness material (16 of Tonti) to have different thicknesses within PMOS gates than in NMOS gates. Accordingly, there is no teaching or suggestion within the Examiner's cited references of Tonti and Chau for forming the claim 69 recited CMOS having a metal-containing material within a PMOS gate that is of a greater thickness than a metal-containing material within an NMOS gate.

Applicant notes that the Examiner's other cited references do not cure the above-described defect of Tonti and Chau for failing to disclose the claim 69 recited CMOS

structure having a metal-containing material within a PMOS gate that is thicker than a metal-containing material within a NMOS gate. Accordingly, no combination of the Examiner's cited references suggests or discloses the claim 69 recited feature of having a metal-containing material within a PMOS gate that is thicker than a metal-containing material within an NMOS gate, where the NMOS gate and PMOS gate are comprised by a common CMOS. The references thus do not suggest or disclose all of the recited features of claim 69, and for at least this reason claim 69 is allowable over the cited references. Applicant therefore requests formal allowance of claim 69 in the Examiner's next action.

Claims 70-80 depend from claim 69, and are therefore allowable for at least the reasons discussed above regarding claim 69.

Claim 81 is amended to place the claim in independent form. The amended claim incorporates all of the subject matter of claim 69 therein. Claim 81 is therefore allowable for at least the reasons discussed above regarding claim 69.

Claims 69-81 are allowable for the reasons discussed above, and Applicant therefore requests formal allowance of such claims in the Examiner's next action.

Respectfully submitted,

Dated: NOVEMBER 18, 2004

By: _____

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Enclosure: Copy of the Information Disclosure Statement previously filed on 10/4/2004